

## CLAIMS

What is claimed is:

1. A method for manufacturing a semiconductor device, comprising steps of:  
forming a compressively strained SiGe layer on a silicon substrate;  
ion-implanting atoms to form uniformly distributed interstitial dislocation loops in the SiGe layer; and  
annealing to form uniformly distributed misfit dislocations in the SiGe layer.
2. The method of claim 1, wherein the step of forming the SiGe layer comprises a step of epitaxially growing the SiGe layer on the silicon substrate.
3. The method of claim 2, wherein the SiGe layer is formed at a thickness of approximately 100 Å to 10000 Å.
4. The method of claim 1, further comprising a step of forming a tensilely strained silicon layer on the SiGe layer.
5. The method of claim 1, wherein the step of ion-implanting the atoms causes end-of-range damage in the SiGe layer.

6. The method of claim 1, wherein the step of ion-implanting the atoms causes an amorphous layer to be formed in a surface portion of the SiGe layer.
7. The method of claim 1, wherein the atoms are Ge or Si.
8. The method of claim 1, wherein the atoms are ion-implanted at an implantation concentration of approximately  $1 \times 10^{14}$  atoms/cm<sup>2</sup> to  $1 \times 10^{16}$  atoms/cm<sup>2</sup> at implantation energy of approximately 5 KeV to 100 KeV.
9. The method of claim 1, wherein the step of annealing is formed at a temperature of approximately 500° C to 1100° C for approximately 1 second to 30 minutes.
10. The method of claim 1, wherein density of the interstitial dislocation loops is approximately  $1 \times 10^5$  loops/cm<sup>2</sup> to  $1 \times 10^{12}$  loops/cm<sup>2</sup>.
11. The method of claim 10, wherein density of the misfit dislocations is approximately  $1 \times 10^5$  #/cm<sup>2</sup> to  $1 \times 10^{12}$  #/cm<sup>2</sup>.
12. A method for forming a semiconductor substrate, comprising the steps of:

forming a SiGe layer on a silicon substrate, wherein the SiGe layer is compressively strained;

controllably ion-implanting atoms onto the SiGe layer causing uniformly distributed end-of-range damage therein;

annealing to form interstitial dislocation loops uniformly distributed in the SiGe layer, wherein the uniformly distributed interstitial dislocation loops nucleate uniformly distributed misfit dislocations in the SiGe layer; and

forming a tensilely strained silicon layer on the SiGe layer.

13. The method of claim 12, wherein the step of ion-implanting the atoms causes an amorphous layer to be formed in a surface portion of the SiGe layer.

14. The method of claim 12, wherein the atoms are Ge or Si.

15. The method of claim 12, wherein the atoms are ion-implanted at an implantation concentration of approximately  $1 \times 10^{14}$  atoms/cm<sup>2</sup> to  $1 \times 10^{16}$  atoms/cm<sup>2</sup> at implantation energy of approximately 5 KeV to 100 KeV.

16. The method of claim 12, wherein the step of annealing is formed at a temperature of approximately 500° C to 1100° C for approximately 1 second to 30 minutes.

17. A semiconductor device comprising:
- a silicon substrate;
  - a relaxed SiGe layer formed on the silicon substrate, said SiGe layer including uniformly distributed misfit dislocations; and
  - a tensilely strained silicon layer formed on the relaxed SiGe layer.
18. The method of claim 17, wherein density of the misfit locations in the SiGe layer is approximately  $1 \times 10^5$  loops/cm<sup>2</sup> to  $1 \times 10^{12}$  loops/cm<sup>2</sup>.
19. The method of claim 17, wherein the misfit dislocations are arranged in a shape of grid when viewed from above.
20. The method of claim 17, wherein the SiGe layer is formed at a thickness of approximately 100 Å to 10000 Å.